ABSTRACT OF THE DISCLOSURE

The present invention relates to a ferroelectric non-volatile memory. The configuration of the memory includes: a plurality of ferroelectric capacitors for memory in which each one end is connected to each of a plurality of first bit lines via switching transistor; first plate lines connected to the other ends of the ferroelectric capacitors for memory; first ferroelectric capacitors for reference in which each one end thereof is connected to a second bit line via first n-channel MOS transistor; a second plate line connected to the other ends of the first ferroelectric capacitors for reference; and a p-channel MOS transistor connected to the second plate line.